REMARKS

The Final Office Action mailed March 21, 2003, has been received and reviewed. Claims 1 through 26, and 72 through 106 are currently pending in the application. Claims 1 through 26, and 72 through 106 stand rejected. Applicant proposes to amend claims 1, 72, 103 and 105 and cancel claim 83. Reconsideration is respectfully requested.

Information Disclosure Statement

Applicant notes the filing of a Supplemental Information Disclosure Statement herein on February 11, 2003 and note that no copy of the PTO-1449 was returned with the outstanding Office Action. Applicant respectfully requests that the information cited on the PTO-1449 (which is the same as that of record to that date in the parent application hereto) be made of record herein.

35 U.S.C. § 102(e) Anticipation Rejections

Anticipation Rejection Based on U.S. Patent No. 5,879,957 to Joo

Claims 72 and 79 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Joo (U.S. Patent No. 5,879,957). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Joo discloses a method of forming a capacitor comprising forming an oxide layer 42 on a silicon substrate 54 and filling a contact hole 43 within the oxide layer 42 with a polysilicon plug 44. An optional diffusion layer 53 (TiN, TiW or TaN) is formed over the plug 44 and regions of the surface of oxide layer 42 that are located adjacent thereto. A ruthenium layer 45 is formed over the diffusion layer 53, if any, as well as over the plug 44 and regions of the oxide

layer 42 that are located adjacent to the plug 44. A first ruthenium oxide layer 46 is formed on the ruthenium layer 45 and a platinum layer 47 is formed thereover. The structure is patterned and etched to form a multilayer structure comprising the ruthenium layer 45, ruthenium oxide layer 46 and platinum layer 47. (Joo, Fig. 8E.) The sides of the ruthenium layer 45 are oxidized to form a second ruthenium oxide pattern 49. A second platinum layer is deposited over the entire structure and etched to create platinum sidewalls 50 on the first and second ruthenium oxide 46a, 49 and platinum layer 47a. A dielectric layer 51 and upper platinum layer 52 are deposited thereover. (Joo, Col. 5, line 56- Col. 6, line 53.)

By way of contrast with Joo, claim 72 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising: providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer; creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal; removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer."

Applicant respectfully submits that Joo fails to disclose, either inherently or expressly, every element of claim 72 as proposed to be amended. Specifically, Joo fails to teach creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal. Instead, Joo discloses a ruthenium layer 45 in contact with ruthenium oxide 49, 46.

As Joo fails to disclose, either inherently or expressly, every element of claim 72 as proposed to be amended, claim 72 is not anticipated by Joo.

Claims 73 through 82 and 84 through 102 are each allowable as depending, either directly or indirectly, from allowable claim 72.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on U.S. Patent No. 5,879,957 to Joo

Claims 83 and 84 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Joo (U.S. Patent No. 5,879,957). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.** The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added.)

The discussion of Joo above is incorporated herein. Claim 83 has been canceled and is proposed to be incorporated into independent claim 72. As stated, Joo fails to teach or suggest creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal.

Moreover, one of ordinary skill in the art would not have been motivated to modify the teachings of Joo to substitute aluminum or copper for ruthenium. This is because neither aluminum or copper can be oxidized to form a conductive oxide, as may ruthenium.

Further, the Court of Appeals for the Federal Circuit has stated that "dependent claims are nonobvious under section 103 if the independent claims from which they depend are nonobvious." In re Fine, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). See also MPEP § 2143.03. Having failed to teach or suggest each and every limitation of the current application, the prior art referenced as rendering dependent claim 84 obvious, cannot serve as a basis for rejection.

Obviousness Rejection Based on U.S. Patent No. 6,030,896 to Brown

Claims 1 through 11, 14 through 26, 72 through 89, and 92 through 106 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brown (U.S. Patent No. 6,030,896). Applicant respectfully traverses this rejection, as hereinafter set forth.

Brown discloses a via formed in a semiconductor device. A first layer of dielectric material 10 is deposited on a semiconductor substrate. A first diffusion barrier layer 12 is formed on the dielectric material 10 and a layer of copper 14 is formed thereover. An etch stop/second barrier layer 16 is formed over the layer of copper 14 and a second copper layer 18 is formed thereover. A third barrier layer 20 is formed on the second copper layer 18 and the structure is patterned. A thin layer of conductive material 22 is formed over the third barrier layer 20 and etched to expose the third barrier layer 20. (Brown, FIG. 3.) A second dielectric layer 24 is deposited and planarized to expose third barrier layer 20. (Brown FIG. 4.)

By way of contrast with Brown, independent claim 1 of the presently claimed invention recites a "method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the first dielectric layer; forming a single conducting layer on the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer." Applicant respectfully submits that Brown fails to teach or suggest every element of claim 1 of the presently claimed invention.

Specifically, Brown fails to teach or suggest "forming a single conducting layer on the at least one metal containing barrier layer." Instead, Brown teaches forming a layer of copper 14, a conductive etch stop layer 16, a second layer 18 of copper, and an optional, conductive antireflective barrier diffusion layer 20 over the at least one metal containing barrier layer 12

taught therein. Moreover, Brown lacks any teaching or suggestion of "metal containing spacers on sidewalls of the multilayer structure" that begin "at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer."

As Brown fails to teach or suggest every element of claim 1 of the presently claimed invention, applicant submits that Brown does not render the presently claimed invention obvious.

Claims 2 through 26 are each allowable as depending, either directly or indirectly, from allowable independent claim 1.

Claim 4 is further allowable as Brown fails to teach or suggest forming a second metal containing barrier layer between a first metal containing barrier layer of said at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

Claim 8 is further allowable as Brown fails to teach or suggest forming the single conducting layer comprises forming the single conducting layer of an aluminum-copper alloy.

Claim 12 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a low dielectric constant material.

Claim 13 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a fluorine-doped silicon oxide.

Claim 15 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer by vapor deposition.

Claim 16 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

Claim 17 is further allowable as Brown fails to teach or suggest forming the single conducting layer comprises forming the single conducting layer by vapor deposition.

Claim 18 is further allowable as Brown fails to teach or suggest forming the single conducting layer by CVD, PVD or PECVD.

Claim 22 is further allowable as Brown fails to teach or suggest forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers. Instead, Brown teaches forming the conductive barrier material 22 before the second dielectric layer 24. (Brown, paragraph bridging col. 4 and 5; col. 5, lines 5-17.)

Claims 25 and 26 are further allowable as Brown fails to teach or suggest removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto to expose said single conducting layer. Instead, Brown discloses planarizing the second dielectric layer 24 and conductive barrier material 22 to expose a barrier metal layer 20.

By way of contrast with Brown, claim 72 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising: providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer; creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal; removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer."

Applicant respectfully submits that Brown fails to teach or suggest every element of the claim 72 as proposed to be amended. Specifically, Brown fails to teach or suggest "creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal." Instead, Brown discloses a first copper layer 14 in contact with a metal containing etch stop layer 16. (Brown, col. 4, lines 35-39.) Brown fails to teach or suggest that the etch stop layer 16 comprises at least copper or aluminum as Brown discloses that the etch stop layer 16 "must be both a good etch stop material

during copper etch as well as a good barrier against copper diffusion." Id. Second copper layer 18 is in contact with a metal containing antireflective diffusion barrier 20. (Brown, col. 4, lines 45-49.)

As Brown fails to teach or suggest every element of the presently claimed invention, applicant submits that independent claim 72 of the presently claimed invention is not rendered obvious by Brown. Thus, claim 72 is allowable.

Claims 73 through 82 and 84 through 102 are each allowable as depending, either directly or indirectly, from allowable claim 72.

Claims 73 and 74 are further allowable as Brown fails to teach or suggest forming a second dielectric layer in contact with said single conducting layer. Instead, Brown discloses a dielectric layer 24 in contact with conductive barrier spacers 22 or dielectric layer 25 in contact with etch stop layer 16. (Brown, FIG. 4.)

Claims 75 and 76 are further allowable as Brown fails to teach or suggest forming a metal containing spacer layer on said second dielectric layer and removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto.

Claim 81 is further allowable as Brown fails to teach or suggest forming a second metal containing barrier layer between a first metal containing barrier layer of the at least one metal containing barrier layer and the substrate, said second metal containing barrier layer comprising TiN, TiW, WN, or TaN.

Claim 84 is further allowable as Brown fails to teach or suggest creating the single conducting layer of an aluminum-copper alloy.

Claim 89 is further allowable as Brown fails to teach or suggest forming a second dielectric layer on the single conducting layer to have sidewalls aligned with the conductive layer sidewalls, and forming the metal containing spacer to extend along the sidewalls of the second dielectric layer. Instead Brown discloses a dielectric layer 24 in contact with conductive barrier spacers 22 or dielectric layer 25 on the etch stop layer 16 and above the conductive barrier spacers 22. (Brown, FIGs. 4 and 5.)

Claim 90 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a low dielectric constant material.

Claim 91 is further allowable as Brown fails to teach or suggest forming the second dielectric layer of a fluorine-doped silicon oxide.

Claim 93 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer by vapor deposition.

Claim 94 is further allowable as Brown fails to teach or suggest forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

Claim 95 is further allowable as Brown fails to teach or suggest forming the conducting layer by vapor deposition.

Claim 96 is further allowable as Brown fails to teach or suggest forming the single conducting layer by CVD, PVD or PECVD.

Claim 100 is further allowable as Brown fails to teach or suggest that flanking comprises forming the metal containing spacer by forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first dielectric layer and a top portion of said multilayer structure.

Independent claim 103 is allowable for substantially the same reasons as allowable claim 1. By way of contrast with Brown, claim 103 of the presently claimed invention recites a "method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the first dielectric layer; forming a single conducting layer over the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer; removing aligned portions of the second dielectric layer, the single conducting layer, and the at least one metal containing barrier layer to form a multilayer structure; forming metal containing spacers on sidewalls of the multilayer structure; and removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacers laterally adjacent thereto."

Applicant respectfully submits that Brown fails to teach or suggest every element of the presently claimed invention. Specifically, Brown fails to teach or suggest forming a second dielectric layer in contact with the single conducting layer. Brown teaches utilizing an oxide mask on the second copper layer 18 if "the antireflective layer 20 is not utilized. . . ." (Brown, col. 4, lines 50-62.) The second copper layer 18 is not, however, a single conducting layer over the barrier layer 12 of Brown. Rather, Brown also teaches that a first copper layer 14 and a conductive hard mask 16 are disposed over the barrier layer 12.

Accordingly, as Brown fails to teach or suggest every element of claim 103 of the presently claimed invention, applicant submits that Brown does not render the presently claimed invention obvious.

Claim 104 is allowable as depending from allowable claim 103 of the presently claimed invention.

By way of contrast with Brown, amended claim 105 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising: providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer; creating a conducting layer <u>on</u> the at least one metal containing barrier layer; forming a second dielectric layer on said conducting layer; removing aligned portions of the second dielectric layer, the conducting layer and the at least one metal containing barrier layer to form a multilayer structure; flanking at least one surface of the multilayer structure with a metal containing spacer such that said metal containing spacer is substantially the same height as said second dielectric layer; and removing any remaining portion of the second dielectric layer and upper portions of the metal containing spacer layer laterally adjacent thereto."

Applicant respectfully submits that Brown fails to teach or suggest creating a conductive layer <u>on</u> at least one metal containing barrier layer that overlies a first dielectric layer and forming a second dielectric layer <u>on</u> the conductive layer. Rather, in Brown, the second dielectric layer is formed over a second copper layer 18, which is formed on a conductive diffusion barrier 16 that resides on a first copper layer 14, not on another dielectric layer.

As Brown fails to teach or suggest every element of the presently claimed invention, applicant submits that independent claim 105 of the presently claimed invention is not rendered obvious by Brown. Thus, claim 105 is allowable.

Claim 106 is allowable as depending from allowable claim 105.

Obviousness Rejection Based on U.S. Patent No. 6,277,745 to Liu et al.

Claims 1, 11 through 13, 72 through 75, and 88 through 91 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Liu et al. (U.S. Patent No. 6,277,745). Applicant respectfully traverses this rejection, as hereinafter set forth.

Liu discloses a passivation method of post copper dry etching. Liu discloses a sandwich structure consisting of a bottom barrier layer 4, a copper layer 6 and a top barrier metal layer 8. After formation of this sandwich structure and patterning, the exposed sidewalls are passivated by means of a barrier metal spacer process. Liu teaches that the fully encapsulated copper lines are highly resistant to oxidation which is an otherwise inherent problem with bare copper lines. (Liu, Abstract.)

By way of contrast with Liu, claim 1 of the presently claimed invention recites a method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the first dielectric layer; forming a single conducting layer on the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer.

Applicant respectfully submits that Liu fails to teach or suggest every element of the presently claimed invention. Specifically, Liu fails to teach or suggest forming a single conducting layer on the at least one metal containing barrier layer and forming a second

dielectric layer in contact with the single conducting layer. Instead, Liu teaches an overlying barrier metal layer 8 between a copper conducting layer 6 and a hard mask layer 16. Thus, there are two conducting layers 6 and 8 between the barrier layer 4 and the dielectric layer 16 of Liu. Moreover, the copper conducting layer 6 of Liu is not in contact with the dielectric layer 16 thereof.

As Liu fails to teach or suggest every element of independent claim 1, claim 1 is allowable.

Claims 2 through 26 are each allowable as depending, either directly or indirectly, from allowable claim 1.

Claim 11 is further allowable as Liu fails to teach or suggest forming the second dielectric layer on the conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Independent claim 72 of the presently claimed invention is allowable for substantially the same reasons as independent claim 1. Claim 72 of the presently claimed invention recites a "method for constructing a metallization structure for a semiconductor device, comprising: providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer; creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper surface of said single conducting layer out of contact with any metal; removing aligned portions of the single conducting layer and at least one metal containing barrier layer to form a multilayer structure; and flanking at least one surface of the multilayer structure with a metal containing spacer, said metal containing spacer extending to substantially the same height as said single conducting layer."

Applicant respectfully submits that Liu fails to teach or suggest "providing a substrate having a first dielectric layer underlying at least one metal containing barrier layer" or "creating a single conducting layer over the at least one metal containing barrier layer, said single conducting layer comprising at least copper or aluminum and comprising an upper surface, said upper

surface of said single conducting layer out of contact with any metal." Instead, Liu teaches that an upper surface of copper layer 6 is in contact with barrier metal layer 8. Further, Liu discloses spacers 14 extending to barrier metal layer 8 or etch stop layer 16.

As Liu fails to teach or suggest every element of the presently claimed invention, claim 72 is not rendered obvious in view of Liu. Thus, claim 72 is allowable.

Claims 73 through 102 are each allowable as depending, either directly or indirectly, from allowable claim 72.

Claim 73 is further allowable as Liu fails to teach or suggest forming a second dielectric layer in contact with said conducting layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Claim 89 is further allowable as Liu fails to teach or suggest forming the second dielectric layer on the conducting layer to have sidewalls aligned with sidewalls of the conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer. Instead, Liu teaches forming a hard mask layer 16 over a second barrier metal layer 8.

Obviousness Rejection Based on U.S. Patent No. 6,074,943 to Brennan et al.

Claims 1 through 12, and 14 through 24 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Brenna et al. [sic] (U.S. Patent No. 6,074,943). Applicant respectfully traverses this rejection, as hereinafter set forth.

Brennan teaches a method of forming via structures using sidewalls as guides. Thus, as shown in FIGS. 2A-2H, Brennan teaches an Al-Cu layer 210 overlying an oxide layer 200 and an optional TiN barrier layer 205. A layer of anti-reflective coating (TiN) 215 is deposited on the Al-Cu layer 210. A layer of sidewall material 240 is deposited (FIG. 2E) and etched to an etch stop layer 220. The etch stop layer 220 is removed and a dielectric material 250 is deposited over the structure in contact with and sidewalls 240. (FIG. 2G.) Brennan teaches that after the dielectric material 250 deposition is complete, "the sidewall material 240 will jut up into the ILD 250, forming sidewall extensions 260." (Brennan, col. 2, lines 64-66.) Subsequently, vias 270 are etched in the ILD layer 250 to contact the underlying interconnect. (FIG. 2H.)

Applicant respectfully submits that Brennan fails to teach or suggest every element of the presently claimed invention. By way of contrast with Brennan, claim 1 of the presently claimed invention recites a "method for making a metallization structure for a semiconductor device, comprising: forming a substantially planar first dielectric layer on a substrate; forming at least one metal containing barrier layer over the first dielectric layer; forming a single conducting layer on the at least one metal containing barrier layer; forming a second dielectric layer in contact with the single conducting layer; removing aligned portions of the second dielectric layer, single conducting layer, and at least one metal containing barrier layer to form a multilayer structure; and forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer."

Applicant respectfully submits that Brennan fails to teach or suggest "forming a single conducting layer on the at least one metal containing barrier layer," "forming a second dielectric layer in contact with the single conducting layer" and "forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer."

The Examiner considers the PETEOS layer 200 of Brennan to be equivalent to the second dielectric layer and the anti-reflective layer 215 to be equivalent to the conducting layer. Even assuming this correlation is correct, which applicant does not concede, Brennan fails to teach or suggest "forming metal containing spacers on sidewalls of the multilayer structure, said metal containing spacers beginning at a lower surface of said at least one metal containing barrier layer and extending substantially to an upper surface of said second dielectric layer."

As Brennan fails to teach or suggest every element of claim 1 of the presently claimed invention, applicant respectfully submits that claim 1 is not rendered obvious by Brennan. Accordingly, claim 1 is allowable.

Claims 2 through 26 are each allowable as depending, either directly or indirectly from allowable claim 1.

Claim 2 is further allowable as Brennan fails to teach or suggest forming a silicon oxide or BPSG layer.

Claim 11 is further allowable as Brennan fails to teach or suggest forming a second dielectric layer comprises forming the second dielectric layer on the single conducting layer to have sidewalls aligned with sidewalls of the single conducting layer, and forming the metal containing spacers to extend along the sidewalls of the second dielectric layer.

Claim 15 is further allowable as Brennan fails to teach or suggest forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by vapor deposition.

Claim 16 is further allowable as Brennan fails to teach or suggest forming the at least one metal containing barrier layer comprises forming the at least one metal containing barrier layer by CVD, PVD or PECVD.

Claim 17 is further allowable as Brennan fails to teach or suggest forming the single conducting layer comprises forming the single conducting layer by vapor deposition.

Claim 18 is further allowable as Brennan fails to teach or suggest forming the single conducting layer by CVD, PVD or PECVD.

Claim 22 is further allowable as Brennan fails to teach or suggest forming the metal containing spacers comprises forming a metal containing spacer layer over the multilayer structure and first dielectric layer and removing portions thereof overlying the first and second dielectric layers.

ENTRY OF AMENDMENTS

The proposed amendments to the claims above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1-26, 72-82 and 84-106 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned attorney.

Respectfully submitted,

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